REMARKS

I. Introduction

Applicants acknowledge with appreciation the indication of allowance of claim 33, and the indication of allowable subject matter being recited by claims 5, 10, 12, 31-32 and 34-35. In response to the Office Action mailed April 20, 2004, Applicants have amended claims 1, 8, 10-11 and 31-34 so as to address the pending claim objection and the rejection under 35 U.S.C. § 112, second paragraph, in a manner suggested by the Examiner during our telephonic interview conducted on May 3, 2004.

Moreover, under the present practice, second or any subsequent actions on the merits shall be made final, except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an IDS (see, **M.P.E.P. § 706.07**).

In the instant case, the Examiner has rejected claim 10 under a new ground of rejection under 35 U.S.C. § 112, second paragraph, where claim 10 was previously indicated to be allowable in the Office Action dated August 13, 2003. Since the new ground of rejection to claim 10 is not necessitated by applicants' amendment (see, "Amendment" dated November 13, 2003), Applicants respectfully request that the finality to the instant application be withdrawn.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 112, Second Paragraph

Claims 8, 10, 12, 31-32 and 34 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

With regard to the failure to adequately describe "a substrate made of resin having a penetration hole, the penetration hole is formed at a position according to a matrix," this language has been deleted from the claims, and has essentially been replaced with the phrase "a substrate having penetration holes, wherein said penetration holes are formed at positions according to a matrix" in an effort to clarify the subject matter of the present invention.

Furthermore, the Examiner asserts that it is not understood what "at positions according to a matrix" refers to. However, as readily shown, for example, in Fig. 3(a) of Applicants' drawings, a plurality of penetration holes form a NxM matrix, or in this instance, a 6-by-6 matrix of aligned rows and aligned columns. Accordingly, each of the penetrations holes is formed precisely at a location or position according to a predetermined matrix comprising rows and columns. Thereafter, a specific number of chip components are inserted at the positions or locations of these penetration holes. By inserting chip components into these penetration holes formed in accordance with the predetermined matrix, the performance of the automatic chip-inserting machine can be enhanced (see, e.g., page 5-6 of specification).

As such, it is respectfully submitted that the foregoing amendments to the claims, in conjunction with the foregoing explanation, which identifies the relevant portions of the specification that support the claim terms questioned in the pending rejection, remove any

possible indefiniteness in the claims, and thus overcome the pending rejection of the claims under 35 U.S.C. § 112, second paragraph.

III. The Rejection Of The Claims Under 35 U.S.C. § 102(e)

Claim 8 is rejected under 35 U.S.C. § 102(e) as being anticipated by USP No. 5,875,100 to Yamashita. Applicants respectfully traverse this rejection for at least the following reasons.

As recited by claim 8, a module component comprises: 1) circuit wirings disposed on both sides of said substrate, 2) a chip component having a predetermined height being greater than the depth of one of said penetration holes and not projecting from said first and second auxiliary substrate, said chip component electrically coupling said circuit wirings to each other, and 3) wherein said penetration holes are formed at positions according to a matrix.

Turning to the prior art, the penetration hole or recessed portion 21 disclosed in Yamashita, which functions to receive the component 10, does not extend through the entire substrate as recited by the pending claim so as to allow the chip component disposed in the penetration hole to contact circuit wiring disposed on both sides of the substrate. Indeed, nowhere in the disclosure of Yamashita does it disclose or suggest that the chip component has a predetermined height being greater than the depth of one of the penetration holes. As readily shown in Fig. 1A-1G of Yamashita, the component 10 clearly does not have a height being greater than the depth of the recessed portion 21 in the manner asserted by the Examiner. Thus, at a minimum, Yamashita does not disclose or suggest a chip component having a predetermined height being greater than the depth of

one of said penetration holes and not projecting from said first and second auxiliary substrate, as recited by the rejected claim.

Further, claim 8 recites that the chip component electrically couples the circuit wirings disposed on both sides of the substrate. However, the component 10 of Yamashita only couples the circuit wirings 22 disposed on a **single side** of the printed circuit board 20. Thus, at a minimum, Yamashita does not disclose or suggest that a chip component electrically couples the circuit wirings disposed on **both sides** of the substrate, as recited by claim 8.

Moreover, nowhere in the disclosure does Yamashita disclose or suggest that the recessed portions are formed at positions according to a matrix. Thus, at a minimum, Yamashita fails to disclose or suggest that the penetration holes are formed at positions according to a matrix, as recited by claim 8.

As anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for the foregoing reasons, it is clear that Yamashita does not anticipate claim 8.

IV. The Rejection Of The Claims Under 35 U.S.C. § 103(a)

Claims 1, 4, 6-7 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over USP No. 4,979,076 to DiBugnara in view of USP No. 4,933,808 to Horton. Applicants respectfully traverse this rejection for at least the following reasons.

In accordance with the present invention and as discussed above, by forming the penetration holes according to a predetermined matrix, chip components can be

automatically inserted into the penetration holes by a machine efficiently. As a result, performance of the inserting machine is enhanced, thereby realizing size-reduction of the chip components and pitch narrowing of the penetration holes.

Turning to the prior art, the Examiner asserts that DiBugnara discloses that each of the penetration holes is aligned in both a row and a column of a matrix. However, as shown in Figs. 1, 2 and 4, it is clear that the apertures 10-19 are not aligned in the manner asserted by the Examiner. Indeed, the opposite is true in that the apertures are arranged on the basis of design needs, and does not necessarily generate any row or column. Thus, at a minimum, DiBugnara does not disclose or suggest that each of the penetration holes are aligned in both a row and a column of a matrix, as currently recited by claim 1.

Furthermore, the Examiner admits that DiBugnara fails to teach "a matrix of N aligned rows and M aligned columns of said penetration holes, wherein N is equal to or greater than three, and M is equal to or greater than three," and relies upon Horton to cure this deficiency. The Examiner's motivation for making the proposed combination is "to easily assemble more components, save less time and low cost for manufacturing (see, page 6, lines 8-9 of Office Action)."

However, this cited motivation for combining the references is flawed. Specifically, there does not appear to be any suggestion in DiBugnara that the printed circuit board disclosed therein cannot be assembled with "more components" as asserted by the Examiner. In fact, DiBugnara discloses that "the dimensions of the board can be left to the designer's discretion (see, col. 4, line37-39)," which translates into an increase in the number of components for a larger size of the printed board. Indeed, DiBugnara discloses that providing a fast and economical method for manufacturing the integrated circuit is the

object of the invention (see, col. 2, lines 39-43). Accordingly, there is simply no motivation to make the proposed modification of DiBugnara with the teachings of Horton absent reference to the Applicants' claimed invention, which is clearly impermissible. That is, the proposed combination is improperly based solely on improper hindsight reasoning, whereby the Examiner selected bits and pieces of the prior art and used only Applicants' specification as a guide to reconstruct the claimed invention. Indeed, the alleged motivation asserted by the Examiner for "forming a matrix where N and M are equal to or greater than three" is found in neither DiBugnara nor Horton. As such, one of ordinary skill in the art would not have combined the teachings of DiBugnara and Horton in the manner alleged by the Examiner to arrive at the claimed invention.

Accordingly, neither DiBugnara nor Horton, taken alone or in combination, render claim 1 nor any of the claims dependent thereon as deemed obvious. Thus, for at least the foregoing reasons, it is respectfully submitted that the combination of DiBugnara and Horton is improper, and therefore the withdrawal of the pending rejection is respectfully requested.

V. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as

claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

For all of the foregoing reasons, it is submitted that claims 4, 6-7 and 9 are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections of claims 4, 6-7 and 9 under 35 U.S.C. § 103 be withdrawn.

Furthermore, with regard to claim 11, the Examiner has not expressly addressed the claim elements recited by the foregoing claim. Indeed, it does not appear that the cited prior art references disclose or suggest a ground layer disposed beneath the substrate, the ground layer being coupled with one of the circuit wirings disposed on a lower side of the substrate. As such, it is respectfully submitted that claim 11 is patentable over the cited prior art.

VI. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 MEF/AHC
Facsimile: (202) 756-8087
Date: June 23, 2004